REMARKS/ARGUMENTS

Claims 1 - 20 are pending in this application. Claims 1 - 20 are rejected. Claim 2 has been amended. No new matter has been added. In view of the amendments and the following remarks, reconsideration and allowance of all pending claims are respectfully requested.

Rejection of Claims under 35 U.S.C. § 103

Claims 1 - 4, 6-11, 13-18, 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Machida et al., U.S. 6046492, (hereinafter Machida) in view of Kunst. The Applicants respectfully traverse the rejection. Claim 2 has been rewritten in independent form to clarify the invention and not to overcome any basis of rejection. No new mater has been added. In view of this amendment, Applicants respectfully submit that no new search is required. The rejection of claims 1 – 20 under 35 U.S.C. §103(a) is believed to be overcome and notice to that effect is requested.

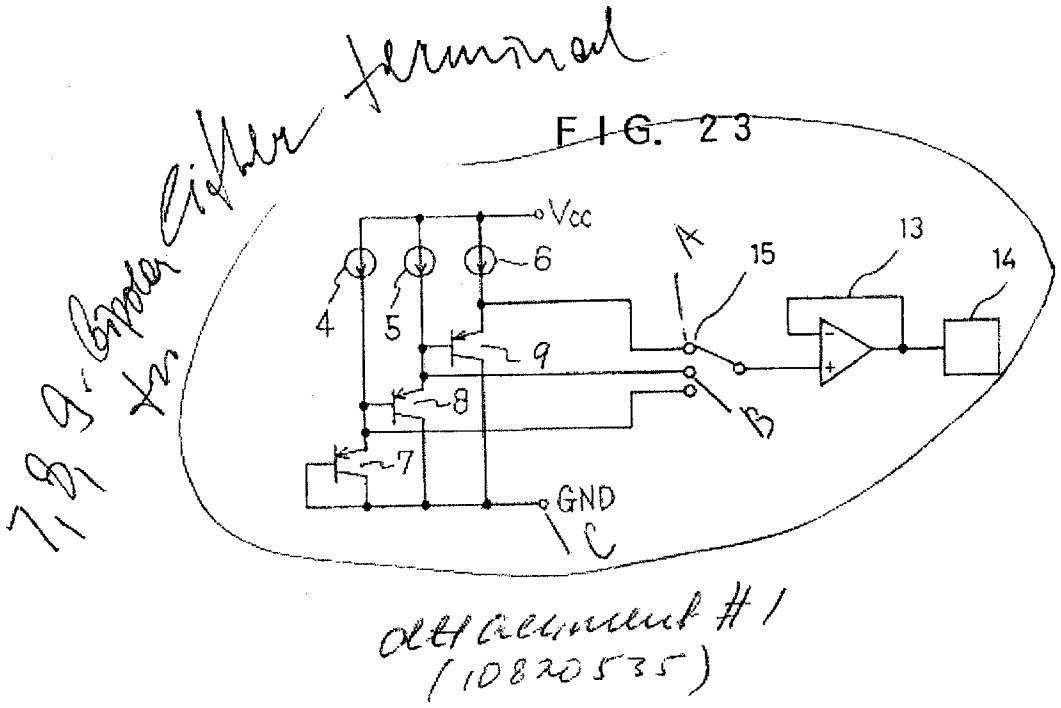
Claim 1 recites at least the following limitations not described, taught or otherwise suggested by any of the cited references:

> "a dual ***diode*** system, comprising a first junction diode and a second junction ***diode*** wherein the first junction diode and the second junction diode are collocated on a first substrate, the dual diode system having a ***first terminal that is coupled to a first electrode of the first junction diode***, wherein the first electrode of the first junction diode has a ***first polarity***, ***a second terminal that is coupled to a first electrode of the second junction diode***, wherein the first electrode of the second junction diode has the ***first polarity***, and ***a third terminal that is coupled to second electrodes of the first and second junction diodes***, wherein the second electrodes of the first and second junction diodes have a second polarity that is ***opposite of the first polarity***"

The Office Action states "Machida discloses in Fig. 23 a device comprising a temperature sensor having two (three) transistors1 junction diodes (collocated on the same substrate1

support) whose first electrode is connected to a first terminal A, a second electrode B is connected to a third terminal C (Vgroundl Vbias), wherein only one of the first and second terminals A, B is connected to a measurement circuit 13 (and pad 14) by means of a switch 15. It is inherent, that the third terminal is used for temperature measurements (The numerals A-C have been added by the Examiner, see attachment # 1 to the Office Action)." (Office Action, p. 2).

In addition, the Office Action attached the following figure:



(Office Action, Attachment 1).

Machida does not teach diodes coupled between electrodes.

As is explained in the Office Action and illustrated in the attachment 1, Machida does not teach a dual ***diode*** system. Machida teaches a first transistor 9 coupled between a first electrode A and a third electrode C. The emitter of the first transistor 9 is coupled to the first electrode A and the collector of the first transistor 9 is coupled to the third electrode C. ***The emitter and the***

collector of the first transistor 9, however, do not form a diode. For example, a diode may be formed either between the emitter and the base of the transistor, or between the collector and the base. The connection across the emitter and collector of the first transistor 9, however, is not a diode junction. Transistor 9 is a PNP type of Bipolar Junction Transistor (BJT), where the positively doped material (or P-type material) is used for the emitter and collector areas of the transistor, and where the negatively doped material (or N-type material) is used for the base region of the transistor. The collector and emitter regions of a PNP transistor are of the ***same material type,*** namely the P-type material. It is well understood that a ***diode*** can only be formed at the interface of a ***PN*** junction, where N-type material and P-type material come together. Since both the collector and the emitter each correspond to P-type material, there is no diode junction formed between terminal A and terminal C (terminal A is P-type material and terminal C is also P-type material). Accordingly, Machida fails to teach a junction diode between the first electrode A and the third electrode C, as is only found in Applicants claim 1.

Similar to transistor 9, Machida also illustrates a second transistor 8 coupled between a second electrode B and a third electrode C. The emitter (or P-type material) of the second transistor 8 is coupled to the second electrode B and the collector (also P-type material) of the second transistor 8 is coupled to the third electrode C. The emitter and the collector of the second transistor 8, however, do not form a diode. For example, a diode may be formed either between the emitter (P-type material) and the base (N-type material) of the transistor 8, or between the collector (P-type material) and the base (N-type material). The connection across the emitter and collector of the second transistor 8, however, is not a diode (see discussion

above). Accordingly, a junction diode is not coupled between the second electrode B and the third electrode C, as is only found in Applicants claim 1.

Machida does not teach electrodes coupled to regions of opposite polarities.

The first electrode A is coupled to the emitter of the first transistor 9 while the third electrode C is coupled to the collector of the first transistor 9. Both ***the emitter and the collector*** of PNP transistor 9, however, are P-type material regions for transistor 9 which ***have the same polarity***. Accordingly, the first electrode A and the third electrode C are not coupled to regions of opposite polarities (as they would be if they were coupled across a PN junction, or diode).

Similarly, the second electrode B is coupled to the emitter of the second transistor 8 while the third electrode C is coupled to the collector of the second transistor 8. Both the emitter and the collector of PNP transistor 8, however, are P-type material regions. These regions have the same polarity. Accordingly, the second electrode B and the third electrode C are not coupled to regions of opposite polarities (as they would be if they were coupled across a PN junction, or diode).

Simply stated, Machida neither teaches coupling terminals across diode junction or coupling terminals to regions of opposite polarity as is found in Applicants claim 1. Since Machida does not teach or suggest "a dual diode system, comprising a first junction diode and a second junction diode wherein the first junction diode and the second junction diode are collocated on a first substrate, the dual diode system having a first terminal that is coupled to a first electrode of the first junction diode, wherein the first electrode of the first junction diode has a first polarity, a second terminal that is coupled to a first electrode of the second junction diode, wherein the first electrode of the second junction diode has the first polarity, and a third terminal

that is coupled to second electrodes of the first and second junction diodes, wherein the second electrodes of the first and second junction diodes have a second polarity that is opposite of the first polarity" as is recited in Claim 1, Claim 1 is proposed to be allowable. Claims 3 – 7 are proposed to be allowable as they depend from a valid base claim. Therefore a notice of allowance is requested with respect to claims 1 and 3 – 7.

As amended, Claim 2 recites in part:

> "a dual ***diode*** system, comprising a first junction diode of a first transistor and a second junction diode of a second transistor; wherein the first transistor and the second transistor are collocated on a first substrate, the first transistor and the second transistor are of a same transistor type, the dual diode system having ***a first terminal coupled to an emitter of the first transistor, a second terminal coupled to an emitter of the second transistor, and a third terminal coupled in common with a base of the first transistor and a base of the second transistor***"

As discussed above with respect to claim 1, Machida teaches coupling terminals across the emitter and collector of transistors. Machida does not teach coupling terminals across emitters and base regions as is described in Applicant amended claim 2. Further, Machida fails to teach or suggest coupling terminals across a diode junction.

Since Machida does not teach a dual diode system, comprising a first junction diode and a second junction diode wherein the first junction diode and the second junction diode are collocated on a first substrate, the dual diode system having a first terminal that is coupled to a first electrode of the first junction diode, wherein the first electrode of the first junction diode is coupled to a collector of a first transistor and has a first polarity, a second terminal that is coupled to a first electrode of the second junction diode, wherein the first electrode of the second junction diode is coupled to a collector of a second transistor has the first polarity, and a third terminal that is coupled to second electrodes of the first and second junction diodes, wherein the

second electrodes of the first and second junction diodes are coupled, respectively, to bases of the first and second transistors and have a second polarity that is opposite of the first polarity, Claim 2 is proposed to be allowable. Therefore a notice of allowance is requested with respect to Claim 2.

Claim 8 recites in part:

> "collocating a dual ***diode*** system on a first substrate wherein the dual diode system comprises a first terminal that is coupled to a first electrode of a first junction diode, wherein the first electrode of the first junction diode has a first polarity, a ***second terminal that is coupled to a first electrode of a second junction diode***, wherein the ***first electrode of the second junction diode has the first polarity***, and a ***third terminal that is coupled to second electrodes of the first and second junction diodes***, wherein the second electrodes of the first and second junction diodes have a second polarity that is ***opposite of the first polarity***"

As discussed above with respect to claim 1, Machida teaches coupling terminals across the emitter and collector of transistors. Machida neither teaches coupling terminals across diode junctions or coupling terminals to regions of opposite polarity as is described in Applicant's Claim 8. Since Machida does not teach or suggest collocating a dual diode system on a first substrate wherein the dual diode system comprises a first terminal that is coupled to a first electrode of a first junction diode, wherein the first electrode of the first junction diode has a first polarity, a second terminal that is coupled to a first electrode of a second junction diode, wherein the first electrode of the second junction diode has the first polarity, and a third terminal that is coupled to second electrodes of the first and second junction diodes, wherein the second electrodes of the first and second junction diodes have a second polarity that is opposite of the first polarity, Claim 8 is proposed to be allowable. Claims 9 - 14 are proposed to be allowable as they depend from a valid base claim. Therefore, a notice of allowance is requested for Claims 8 – 14.

Claim 15 recites in part:

> "a dual ***diode*** system comprising a first junction diode means and a second junction ***diode*** means wherein the first junction diode means and the second junction diode means are collocated on a first substrate wherein the dual diode system comprises a ***first terminal that is coupled to a first electrode*** of the first junction diode means, wherein the first electrode of the first junction diode means has ***a first polarity***, a ***second terminal that is coupled to a first electrode*** of the second junction diode means, wherein the first electrode of the second junction diode means has the ***first polarity***, and a ***third terminal that is coupled to second electrodes of the first and second junction diode means***, wherein the second electrodes of the first and second junction diode means have a second polarity that is ***opposite of the first polarity***"

As discussed above with respect to claim 1, Machida teaches coupling terminals across the emitter and collector of transistors. Machida neither teaches coupling terminals across diode junctions or coupling terminals to regions of opposite polarity as is described in Applicant's Claim 15. Since Machida does not teach or suggest a dual diode system comprising a first junction diode means and a second junction diode means wherein the first junction diode means and the second junction diode means are collocated on a first substrate wherein the dual diode system comprises a first terminal that is coupled to a first electrode of the first junction diode means, wherein the first electrode of the first junction diode means has a first polarity, a second terminal that is coupled to a first electrode of the second junction diode means, wherein the first electrode of the second junction diode means has the first polarity, and a third terminal that is coupled to second electrodes of the first and second junction diode means, wherein the second electrodes of the first and second junction diode means have a second polarity that is opposite of the first polarity, Claim 15 is proposed to be allowable. Claims 16 – 20 are proposed to be allowable as they depend from a valid base claim. Therefore a notice of allowance is requested with respect to Claims 15 – 20.

Conclusion

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicants at the telephone number provided below.

Respectfully submitted,

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